What is Claimed is:

1. A semiconductor device layout inspection method for inspecting formation defects that will occur in wires of a chip layout, wherein the wire formation defects are detected by checking the relationship between the layout of the contact holes in said wires and the layout of said wires.

2. The semiconductor device layout inspection method according to Claim 1, wherein the layout of wires where wire formation defects have been detected is corrected.

3. A semiconductor device layout inspection method for inspecting formation defects that will occur in wires of a chip layout, wherein the wire formation defects are detected by providing limitation to the area ratio of the total area of the wires of the same node to the total area of the contact holes in the wires of the same node of the chip layout so that existence of defects is determined based on this limitation.

4. A semiconductor device layout inspection method for inspecting formation defects that will occur in wires of a chip layout, wherein the wire formation defects are detected by providing limitation to the number of contact holes in the wires of the same node so that existence of defects is determined based

on this number limitation.

5. A semiconductor device layout inspection method for inspecting formation defects that will occur in wires of a chip layout, wherein the wire formation defects are detected by providing limitation to the number of contact holes in the wires having a constant width so that existence of defects is determined based on this number limitation.

6. A semiconductor device layout inspection method for inspecting formation defects that will occur in wires of a chip layout, wherein the wire formation defects are detected by providing limitation to the total area of contact holes in the wires having a constant width so that existence of defects is determined based on this area limitation.

7. A semiconductor device layout inspection method for inspecting formation defects that will occur in wires of a chip layout, comprising: the step of calculating the total area of the wires of the same node and the total area of the contact holes in the wires of the same node; and the step of determining the area limitation value of said contact holes in accordance with said total area of the wires of the same node, wherein the area of the same node is detected as a wire formation defect when said total area of the contact holes is equal to, or is

greater than, said area limitation value.

8. A semiconductor device layout inspection method for inspecting formation defects that will occur in wires of a chip layout, comprising: the step of calculating the total area of the wires of the same node and the number of the contact holes in the wires of the same node; and the step of determining the number limitation value of said contact holes in accordance with said total area of the wires of the same node, wherein the area of the same node is detected as a wire formation defect when said number of the contact holes is equal to, or is greater than, said number limitation value.

9. A semiconductor device layout inspection method for inspecting formation defects that will occur in wires of a chip layout, comprising: the step of calculating the number of the contact holes in the wires having a constant width; and the step of determining the number limitation value of said contact holes that varies in accordance with the wire width, wherein the area concerning the contact holes is detected as a wire formation defect when said number of the contact holes is equal to, or is greater than, said number limitation value.

10. A semiconductor device layout inspection method for inspecting formation defects that will occur in wires of a chip

layout, comprising: the step of calculating the total area of the contact holes in the wires having a constant width; and the step of determining the area limitation value of said contact holes that varies in accordance with the wire width, wherein the area concerning the contact holes is detected as a wire formation defect when said total area of the contact holes is equal to, or is greater than, said area limitation value.

11. A semiconductor device layout inspection method for inspecting formation defects that will occur in wires of a chip layout, comprising: the step of dividing the entire area of the chip layout into a plurality of inspection regions; the step of providing limitation to the number of the contact holes in the wires of a constant width in an inspection region from among said plurality of inspection regions so that a wire formation defect is detected by determining the existence of a defect based on this number limitation; and the step of allowing said inspection region to scan the entire surface of the chip layout.

12. The semiconductor device layout inspection method according to Claim 11, wherein the entire surface inspection for inspecting the entire chip surface of the chip layout and a partial inspection for inspecting a portion of the chip have different scanning intervals of the inspection regions.

13. The semiconductor device layout inspection method according to Claim 11, wherein the entire surface inspection for inspecting the entire chip surface of the chip layout and a partial inspection for inspecting a portion of the chip have different sizes of the inspection regions.

14. The semiconductor device layout inspection method according to Claim 5, wherein limitation is provided to the number of the contact holes in wires having a constant width after wires connected to contact holes of which the number is less than a constant number in the chip layout has been removed in advance.

15. The semiconductor device layout inspection method according to Claim 5, wherein limitation is provided to the number of the contact holes in wires having a constant width in inspection regions that have been limited to the inspection regions having contact holes of which the number is equal to, or greater than, a constant number from among the plurality of inspection regions.

16. A semiconductor device layout inspection method for inspecting formation defects that will occur in wires of a chip layout, comprising: the step of dividing the entire area of the

chip layout into a plurality of inspection regions; and the step of providing limitation to the area ratio of the total area of the wires of the same node to the total area of the contact holes in the wires of the same node using an antenna check in an inspection region from among said plurality of inspection regions so that a wire formation defect is detected by determining the existence of a defect based on this limitation; and the step of allowing said inspection region to scan the entire surface of the chip layout.

17. A semiconductor device layout inspection method for inspecting formation defects that will occur in wires of a chip layout, comprising: the step of defining a partial inspection region in the chip layout; the step of providing limitation to the area ratio of the total area of the wires of the same node to the total area of the contact holes in the wires of the same node using an antenna check in said partial inspection region so that a wire formation defect is detected by determining the existence of a defect based on this limitation; and the step of allowing said partial inspection region to scan the entire surface of the chip layout using a density check.